

# 4 Ports HDMI 1.3 Splitter

## EP9134

### User Guide

## V0.8

**Revised: Dec. 05, 2009**

**Original Release Date: Aug. 27, 2007**

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## Revision History

Version Number	Revision Date	Author	Description of Changes
0.0	Aug/27/2007	Jerry Chen	Initial Version
0.1	Jan/11/2008	Ether Lai	Revised Version
0.2	Mar/14/2008	Ether Lai	Revise Register Description; Change package type;
0.3	May/08/2008	Ether Lai	Revise Register Description; Revise Pin Definition; Revise Power Consumption; Change package type to E-PAD LQFP;
0.4	Jul/23/2009	Ether Lai	Remove redundant register descriptions; Clarify HDMI version -- specification and CTS; Revise Package Diagram;
0.5	Aug/18/2009	Ether Lai	Revise Package Diagram to E-PAD;
0.6	Oct/23/2009	Ether Lai	Fix Typo in EXT_SWING pin descriptions;
0.7	Nov/23/2009	Ether Lai	Fix Typo in DC Analogue Specification and Figure 2-3; Fix typo in section 3.1, section 3.2.1, section 3.3.1.7 and table 3-1; Revise the thermal resistance;
0.8	Dec/05/2009	Ether Lai	Fix Typo in Register Description;

# Section 1 Introduction

## 1.1 Overview

The EP9134 is a 4-Port DVI/HDMI splitter with integrated HDCP decryption/encryption engines and is compliant with HDMI Rev 1.3a and HDCP Rev 1.2 specifications. The EP9134 receives DVI/HDMI inputs, process HDCP decryption and encryption and transmits the data to 4 DVI/HDMI ports. The chip uses an external EE to store the encrypted HDCP receiver/transmitter keys.

## 1.2 Features

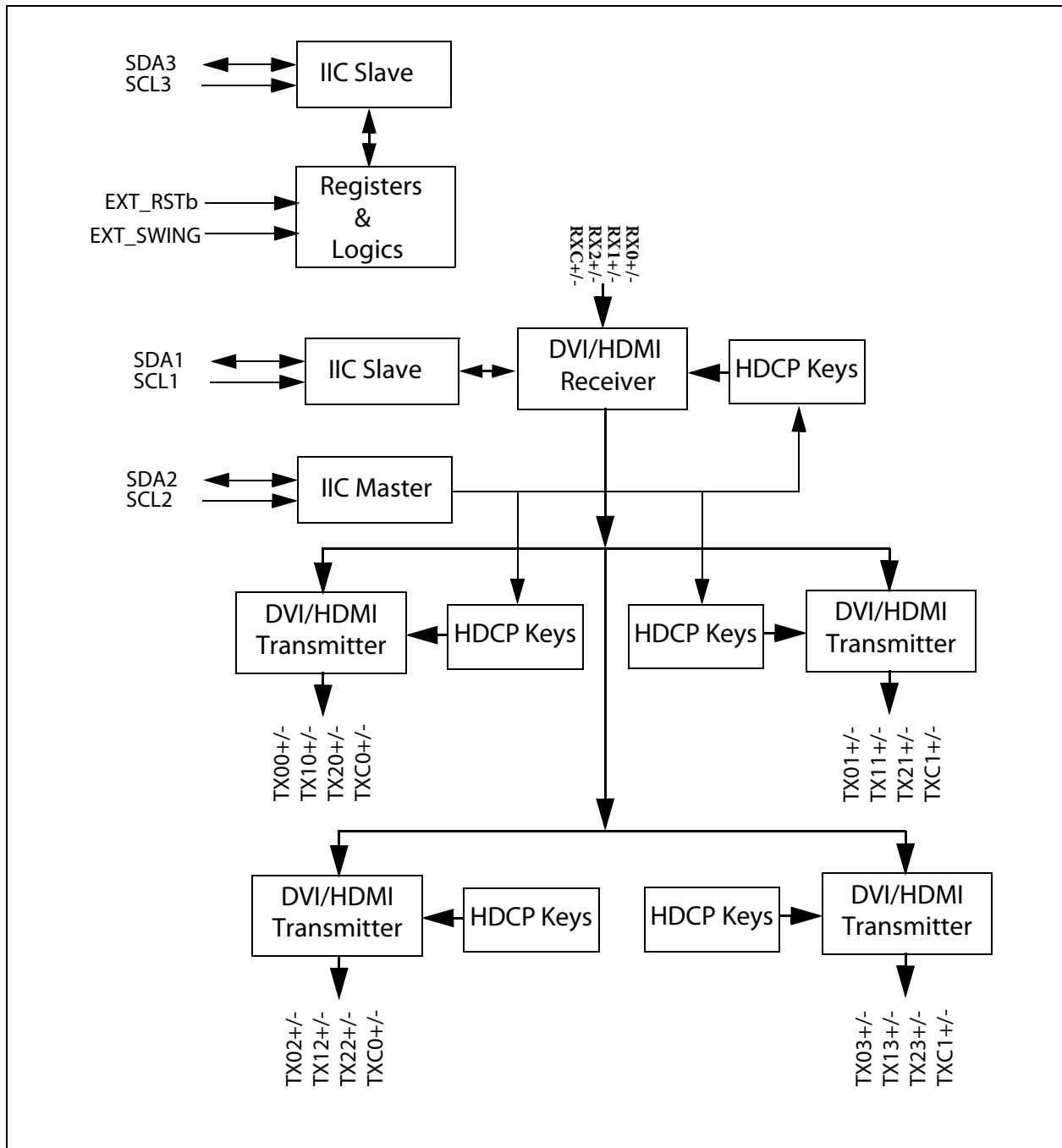
- DVI Specification 1.0 Compliant
- Compliant with HDMI 1.3a specification and HDMI 1.3c Compliance Test Specification (CTS)
- Integrated HDCP decryption/encryption engines which are compliant with HDCP Rev 1.2 specification
- Encrypted HDCP keys store in external serial EE
- Wide Frequency Range: 25MHz - 225MHz
- Support 12-bit Deep Color up to 1080p
- Supports 1 DVI/HDMI input port and 4 DVI/HDMI output ports
- Supports conversion of HDMI signaling to DVI signaling
- Supports HDCP Repeater
- Cascadable to make more than 4 output ports
- 128-Pin E-PAD LQFP (Pb-Free)



## Section 2 Overview

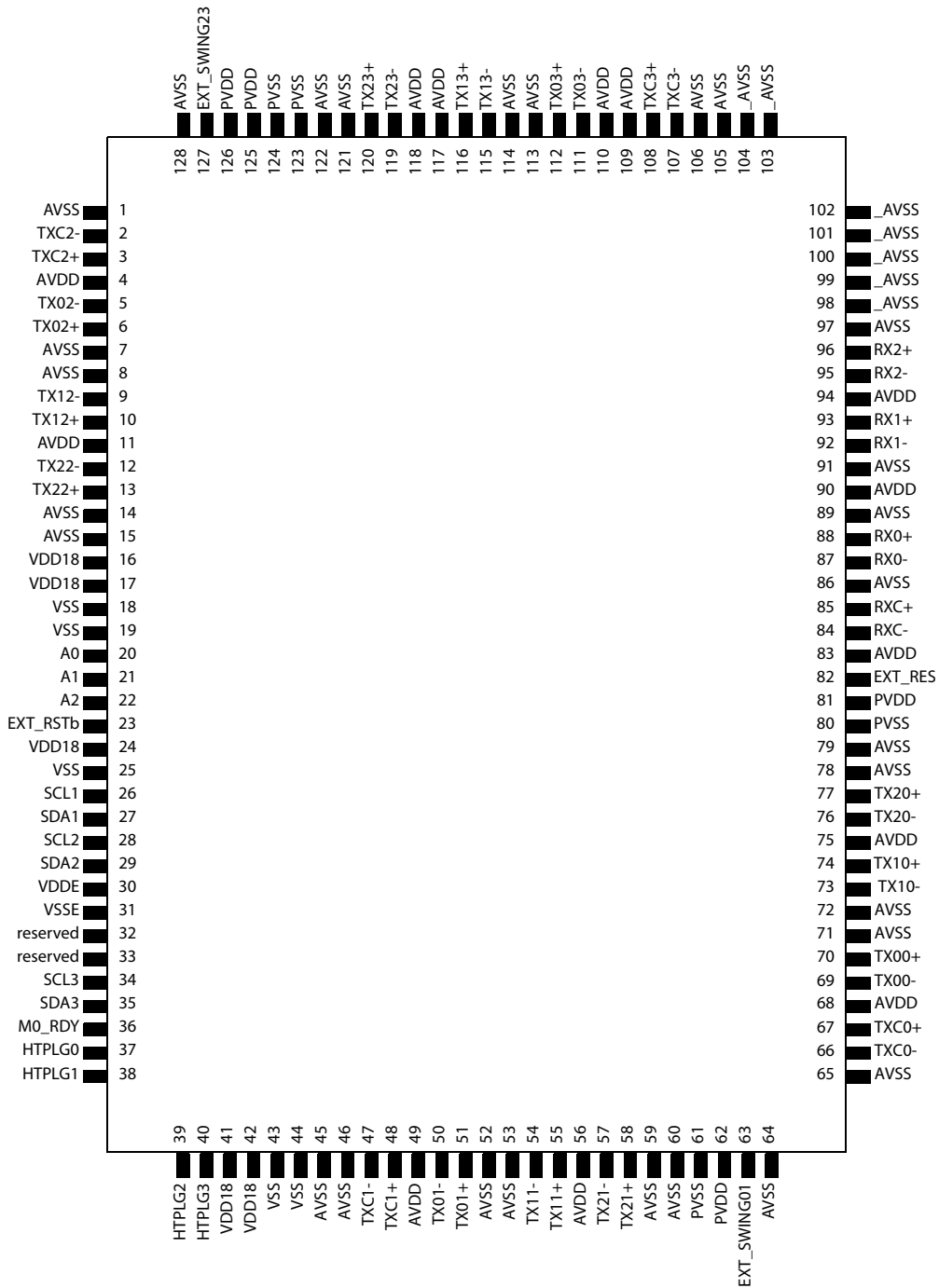
### 2.1 Block Diagram

Figure 2-1 Block Diagram



## 2.2 Pin Diagram

Figure 2-2 Pin Diagram



## 2.3 Pin Description

Unless otherwise stated, unused input pins must be tied to ground, and unused output pins left open.

**Table 2-1 IIC Pins**

NAME	IN / OUT	DESCRIPTION
SCL1	IN	IIC SCL signal for receiver port DDC
SDA1	IO	IIC SDA signal for receiver port DDC (open drain)
SCL2	OUT	IIC SCL signal for EE interface (open drain)
SDA2	IO	IIC SDA signal for EE interface (open drain)
SCL3	IN	IIC SCL signal for internal registers access
SDA3	IO	IIC SDA signal for internal registers access (open drain)
A2, A1, A0	IN	Determine the lowest 3-bit of the IIC address for IIC Port 3 (SCL3/SDA3)

**Table 2-2 Misc. Pins**

NAME	IN / OUT	DESCRIPTION
EXT_RSTb	IN	External Reset (Active LOW). A HIGH level indicates normal operation and a LOW level causes all the logic on the chip to be reset.
M0_RDY	OUT	HDCP M0 Ready Signalling Output. This pin is set to HIGH while the AKSV is written to receiver.
reserved	IN	Must be tied LOW for normal operation.

**Table 2-3 Receiver Pins**

NAME	IN / OUT	DESCRIPTION
RX0- RX0+ RX1- RX1+ RX2- RX2+	Analog	Differential Data Input Pairs for receiver port
RXC- RXC+		Differential Clock Input Pairs for receiver port
EXT_RES	Analog	DVI/HDMI External Termination Resistor.

**Table 2-4 Transmitter Pins**

NAME	IN / OUT	DESCRIPTION
TX00- TX00+ TX10- TX10+ TX20- TX20+	Analog	Differential Data Output Pairs for transmitter port 0
TXC0- TXC0+		Differential Clock Output Pairs for transmitter port 0
HTPLG0	IN	Hot Plug Input This pin is used to monitor the "HOT PLUG" signal for transmitter port 0. Note: This input is only 3.3V tolerant and has no internal debouncer circuit.

**Table 2-4 Transmitter Pins**

NAME	IN / OUT	DESCRIPTION
TX01- TX01+ TX11- TX11+ TX21- TX21+	Analog	Differential Data Output Pairs for transmitter port 1
TXC1- TXC1+		Differential Clock Output Pairs for transmitter port 1
HTPLG1	IN	Hot Plug Input This pin is used to monitor the "HOT PLUG" signal for transmitter port 1. Note: This input is only 3.3V tolerant and has no internal debouncer circuit.
EXT_SWING01	Analog	Voltage Swing Adjust for Port 0/1. A resistor should tie this pin to AVDD. This resistance determines the amplitude of the voltage swing.
TX02- TX02+ TX12- TX12+ TX22- TX22+	Analog	Differential Data Output Pairs for transmitter port 2
TXC2- TXC2+		Differential Clock Output Pairs for transmitter port 2
HTPLG2	IN	Hot Plug Input This pin is used to monitor the "HOT PLUG" signal for transmitter port 2. Note: This input is only 3.3V tolerant and has no internal debouncer circuit.
TX03- TX03+ TX13- TX13+ TX23- TX23+	Analog	Differential Data Output Pairs for transmitter port 3
TXC3- TXC3+		Differential Clock Output Pairs for transmitter port 3
HTPLG3	IN	Hot Plug Input This pin is used to monitor the "HOT PLUG" signal for transmitter port 3. Note: This input is only 3.3V tolerant and has no internal debouncer circuit.
EXT_SWING23	Analog	Voltage Swing Adjust for Port 2/3. A resistor should tie this pin to AVDD. This resistance determines the amplitude of the voltage swing.

**Table 2-5 Power and Ground Pins**

NAME	IN / OUT	DESCRIPTION
VDDE	PWR	Digital Power, 3.3V
VSSE	GND	Digital Ground
VDD18	PWR	Core Power, 1.8V
VSS	GND	Core Ground
AVDD	PWR	Analog Power, 3.3V
AVSS	GND	Analog Ground
PVDD	PWR	Analog Power for PLL, 3.3V
PVSS	GND	Analog Ground for PLL

**Table 2-5 Power and Ground Pins**

NAME	IN / OUT	DESCRIPTION
_AVSS	GND	Analog Ground

## 2.4 Electrical Characteristics

### Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Units
V <sub>CC33</sub>	3.3V Supply Voltage	-0.3		4.0	V
V <sub>CC18</sub>	1.8V Supply Voltage	-0.3		2.5	V
V <sub>I</sub>	Input Voltage	-0.3		V <sub>CC</sub> + 0.3	V
V <sub>O</sub>	Output Voltage	-0.3		V <sub>CC</sub> + 0.3	V
T <sub>J</sub>	Junction Temperature			125	°C
T <sub>STG</sub>	Storage Temperature	-40		125	°C
θ <sub>JA</sub>	Thermal Resistance (Junction to Ambient)		43		°C/W
θ <sub>JC</sub>	Thermal Resistance (Junction to Case)		6		°C/W

1 Permanent device damage may occur if absolute maximum conditions are exceeded.

2 Functional operation should be restricted to the conditions described under Normal Operating Conditions.

### Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V <sub>CC33</sub>	3.3V Supply Voltage	3.14	3.3	3.6	V
V <sub>CC18</sub>	1.8V Supply Voltage	1.71	1.8	1.98	V
V <sub>CCN</sub>	Supply Voltage Noise <sup>1</sup>	-0.3		100	mV <sub>p-p</sub>
T <sub>A</sub>	Ambient Temperature (with power applied)	0	25	70	°C

1 Guaranteed by design.

### DC Digital I/O Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V <sub>IH</sub>	High-level Input Voltage		2.0			V
V <sub>IL</sub>	Low-level Input Voltage				0.8	V
V <sub>OH</sub>	High-level Output Voltage		2.4			V

$V_{OL}$	Low-level Output Voltage				0.4	V
$I_{OL}$	Output Leakage Current	High Impedance	-10		10	uA
$V_{ID}$	Differential Input Voltage		150		1000	mV

### DC Analogue Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{OD}$	Differential Voltage Single ended peak to peak amplitude	$R_{LOAD} = 50 \text{ ohm}$ $R_{EXT\_SWING} = 182 \text{ ohm}$	510	550	590	mV
$V_{DOH}$	Differential High-level Output Voltage <sup>1</sup>			AVDD		V
$I_{DOS}$	Differential Output Short Circuit Current	$V_{OUT} = 0V$ ; TX_TERM bit is 0			5	uA
$I_{PD}$	Power-Down Current <sup>2</sup>	25°C Ambient	3V3		2	mA
			1V8		1	mA
$I_{CCD}$	Supply Current (25°C Ambient, TX0/TX1/TX2/TX3 are Active $R_{EXT\_RES} = 511 \text{ ohm}$ , $R_{EXT\_SWING} = 182 \text{ ohm}$ , TX_TERM bit is 1)	1080p Resolution (8-bit)	3V3		579	mA
			1V8		110	mA
		1080p Resolution (12-bit)	3V3		633	mA
			1V8		161	mA

1 Guaranteed by design.

2 Assumes all HDMI/DVI I/O ports are not connected and all digital inputs are silent.

### Receiver AC Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$T_{DPS}$	Intra-Pair (+ to -) Differential Input Skew <sup>1</sup>				0.4	$T_{bit}$
$T_{CCS}$	Channel to Channel Differential Input Skew <sup>1</sup>				1.0	$T_{pixel}$
$T_{IJT}$	Differential Input Clock Jitter Tolerance <sup>2,3</sup>				0.3	$T_{bit}$
$T_{PDL}$	Delay from OUT_EN Low to High Impedance outputs				10	ns
$T_{HSC}$	Link Disabled (Tx power down) to LINK_ON Low <sup>4</sup>				250	ms
$T_{FSC}$	Link Enabled (DE Active) to LINK_ON High <sup>1</sup>			25	40	DE edges

#### NOTES:

1. Guaranteed by design.

2. Jitter defines as per DVI 1.0 Specification, Section 4.6 *Jitter Specification*.

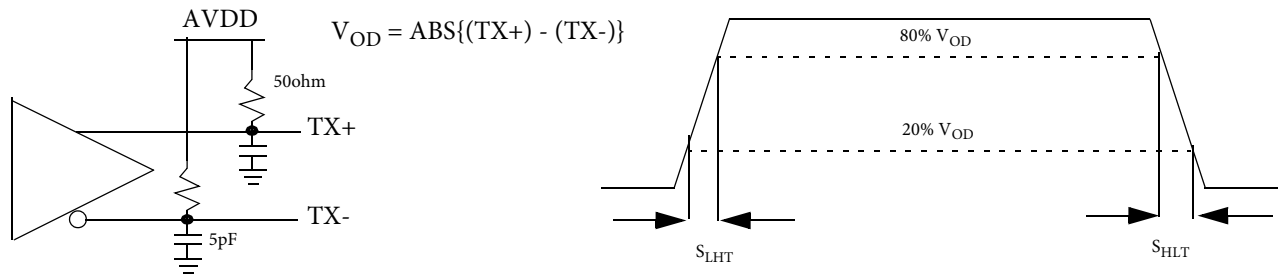
3. Jitter measured with Clock Recovery Unit as per DVI 1.0 Specification, Section 4.7 *Electronical Measurement Procedures*

4. Measured when transmitter was powered down.

**Transmitter AC Specifications** (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$S_{LHT}$	Differential Swing Low-to-High Transition Time	$C_{LOAD} = 5pF$ , $R_{LOAD} = 50\text{ ohm}$ , $R_{EXT\_SWING} = 300\text{ ohm}$	170	200	230	ps
$S_{HLT}$	Differential Swing High-to-Low Transition Time	$C_{LOAD} = 5pF$ , $R_{LOAD} = 50\text{ ohm}$ , $R_{EXT\_SWING} = 300\text{ ohm}$	170	200	230	ps

**Figure 2-3 Differential Output Timing Definition**



## Section 3 Detail Functional Descriptions

### 3.1 General

The chip provides an IIC (SCL3/SDA3) serial bus interface to communicate with the host. The IIC address for this slave IIC interface is "0111\_A2\_A1\_A0\_x" (where x=1 for read and x=0 for write). A2, A1 and A0 are programmable by pins

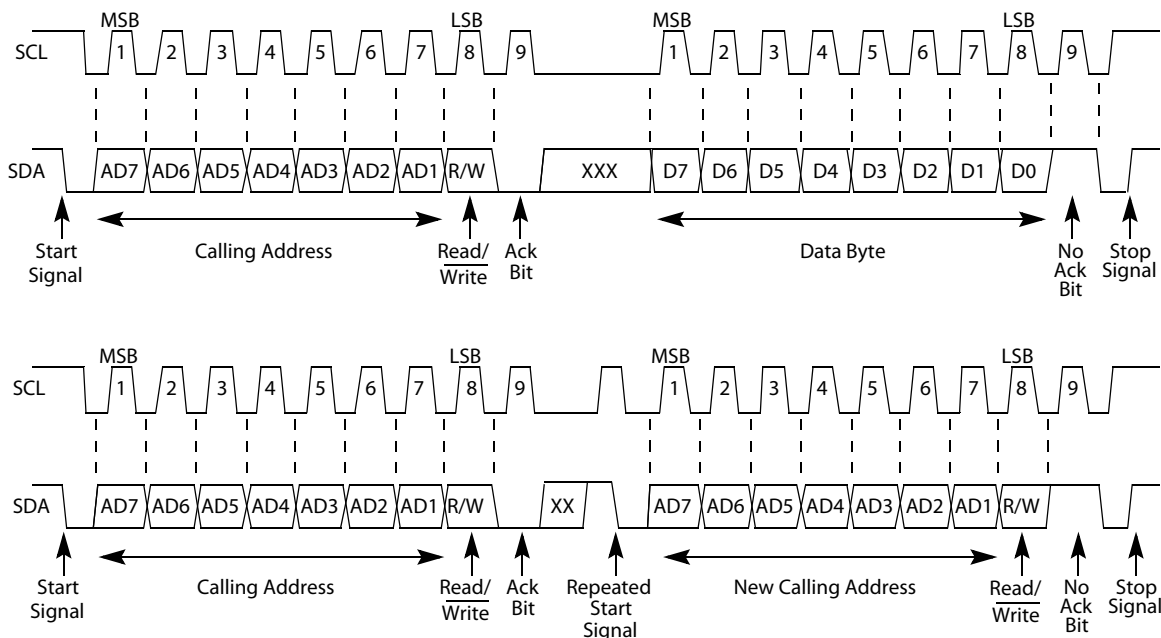
### 3.2 IIC Interface

The IIC bus interface uses a Serial Data line (SDA at pin SDA3) and a Serial Clock Line (SCL at pin SCL3) for data transfer. The chip acts as a slave for receiving and transmitting data over the serial interface. All devices connected to the IIC bus must have open drain or open collector outputs. Logic AND function is exercised on both lines with external pull-up resistors, the value of these resistors is system dependent. When the serial interface is not active, the logic levels on SCL and SDA are pulled HIGH by external pull-up resistors.

Data received or transmitted on the SDA line must be stable at the positive edge of SCL. If the SDA changes state while SCL is HIGH, the IIC interface interprets that action as a START or STOP sequence. Data on SDA must change only when SCL is LOW.

The standard IIC traffic protocol is illustrated in the following Figure:

**Figure 3-1 IIC Bus Transmission Protocol**



### 3.2.1 Basic Protocol

For EP9134, there are six components to serial bus operation:

- START Signal
- Slave Address Byte
- Base Register Address Byte
- Data Byte for Read/Write
- STOP Signal
- Repeated Start Signal

When the serial interface is inactive (SCL and SDA are HIGH), communication are initiated by a START signal which is a HIGH-to-LOW transition on SDA while SCL is HIGH. The first eight bits of data transferred after a START signal comprising a seven bit slave address (the seven MSB bits) and a single R/W bit (the LSB bit). The R/W bit indicates the direction of data transfer, "1" means read from device and "0" means write to device. If the transmitted slave address matches the address of the device, the EP9134 sends the acknowledge by asserting SDA Low on the ninth SCL pulse. Else, the EP9134 does not assert the acknowledge.

Writing data to specific control registers of the chip requires that the 8-bits address of the control register is written after the slave address has been acknowledged. This control register address is the base address for the subsequent write operations. The base address auto-increments by one for each byte of data written after the data byte intended for the base address. The acknowledge bit will be sent on the ninth SCL pulse after every 8-bits data received.

Data are read from the control registers of the chip in a similar manner. Reading requires two data transfer operations:

The base address must be written with the R/W bit of the slave address byte LOW to set up a sequential read operation.

Reading (the R/W bit of the slave address byte HIGH) begins at the previously established base address. The address of the read register auto-increments after each byte is transferred.

To terminate a read/write sequence to the chip, a STOP signal must be sent. A STOP signal comprises a LOW-to-HIGH transition of SDA while SCL is HIGH.

A repeated start signal occurs when the master device driving the serial interface generates a START signal without first generating a STOP signal to terminate the current read/write sequence. This can be used to change the mode of communication (read, write) between the slave and master without releasing the bus.

### 3.2.2 Examples of the read/write sequence

Write to One Control Register

- START Signal
- Slave Address Byte (R/W bit = LOW)

- Base Address Byte
- Data Byte to Base Address
- STOP Signal

#### Write to Multiple Control Registers

- START Signal
- Slave Address Byte (R/W bit = LOW)
- Base Address Byte
- Data Byte to Base Address
- Data Byte to (Base Address + 1)
- Data Byte to (Base Address + 2)
- .....
- Data Byte to (Base Address + N)
- STOP Signal

#### Read from One Control Register

- START Signal
- Slave Address Byte (R/W bit = LOW)
- Base Address Byte
- Repeated START Signal
- Slave Address Byte (R/W = HIGH)
- Data Byte from Base Address
- STOP Signal

#### Read from Multiple Control Registers

- START Signal
- Slave Address Byte (R/W bit = LOW)
- Base Address Byte
- Repeated START Signal
- Slave Address Byte (R/W = HIGH)
- Data Byte from Base Address
- Data Byte from (Base Address + 1)
- Data Byte from (Base Address + 2)
- .....
- Data Byte from (Base Address + N)

- STOP Signal

### 3.3 Description of the Control Registers

The following table shows all the control registers of the DVI/HDMI Transmitter EP9134:

**Table 3-1 IIC Control Registers**

Addr	Mode	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	RESET	
\$05	R/W	-	-	TMDS_SAMP[5:0]							05h
\$06	R/W	TX_TERM	DPRE_EM	TX_BW	TX_PEAK	CPRE_EM	RX_EQ	RX_BW	RX_TERM	00h	
\$07	R/W	RX_LINK_ON	RX_DE_ON	RX_HDMI	RX_ENC_ON	RX_PU	-	TX_SEL[1:0]		08h	
\$08	R/W	TX_MUTE	RX_VSYNC	-	-	-	-	TX_ENC_OPT	TX_PU	01h	
\$09	R	-	-	-	-	-	TX_RSEN	TX_HTPLG	-	00h	
\$0A	R/W	DK[3:1]			DKEN	-	-	-	-	80h	
\$0E	R/W	-	-	-	-	-	-	TX_EESS	TX_HDMI	01h	
\$0F	R/W	TX_AKSV_RDY	TX_ENC_ON	-	TX_RPTR	-	-	TX_RI_RDY	TX_ENC_EN	00h	
\$10	R/W	TX_BKSV_1								XXh	
\$11	R/W	TX_BKSV_2								XXh	
\$12	R/W	TX_BKSV_3								XXh	
\$13	R/W	TX_BKSV_4								XXh	
\$14	R/W	TX_BKSV_5								XXh	
\$15	R/W	TX_AN_1								XXh	
\$16	R/W	TX_AN_2								XXh	
\$17	R/W	TX_AN_3								XXh	
\$18	R/W	TX_AN_4								XXh	
\$19	R/W	TX_AN_5								XXh	
\$1A	R/W	TX_AN_6								XXh	
\$1B	R/W	TX_AN_7								XXh	
\$1C	R/W	TX_AN_8								XXh	
\$1D	R	TX_AKSV_1								XXh	
\$1E	R	TX_AKSV_2								XXh	
\$1F	R	TX_AKSV_3								XXh	
\$20	R	TX_AKSV_4								XXh	

\$21	R	TX_AKSV_5								XXh
\$22	R	TX_RI_1								XXh
\$23	R	TX_RI_2								XXh
\$25	R	TX_M0_1								XXh
\$26	R	TX_M0_2								XXh
\$27	R	TX_M0_3								XXh
\$28	R	TX_M0_4								XXh
\$29	R	TX_M0_5								XXh
\$2A	R	TX_M0_6								XXh
\$2B	R	TX_M0_7								XXh
\$2C	R	TX_M0_8								XXh
\$40	R	0	0	0	0	0	0	0	RX_M0_RDY	00h
\$41	R	RX_M0_1								XXh
\$42	R	RX_M0_2								XXh
\$43	R	RX_M0_3								XXh
\$44	R	RX_M0_4								XXh
\$45	R	RX_M0_5								XXh
\$46	R	RX_M0_6								XXh
\$47	R	RX_M0_7								XXh
\$48	R	RX_M0_8								XXh
\$50	W	RX_Bcaps								91h
\$51	W	RX_Bstatus[7:0]								00h
\$52	W	-	-	-	-	RX_Bstatus[11:8]				00h
\$60	W	RX_SHA-1_HASH_0								XXh
\$61	W	RX_SHA-1_HASH_1								XXh
\$62	W	RX_SHA-1_HASH_2								XXh
\$63	W	RX_SHA-1_HASH_3								XXh
\$64	W	RX_SHA-1_HASH_4								XXh
\$65	W	RX_SHA-1_HASH_5								XXh
\$66	W	RX_SHA-1_HASH_6								XXh
\$67	W	RX_SHA-1_HASH_7								XXh
\$68	W	RX_SHA-1_HASH_8								XXh
\$69	W	RX_SHA-1_HASH_9								XXh

\$6A	W	RX_SHA-1_HASH_10	XXh
\$6B	W	RX_SHA-1_HASH_11	XXh
\$6C	W	RX_SHA-1_HASH_12	XXh
\$6D	W	RX_SHA-1_HASH_13	XXh
\$6E	W	RX_SHA-1_HASH_14	XXh
\$6F	W	RX_SHA-1_HASH_15	XXh
\$70	W	RX_SHA-1_HASH_16	XXh
\$71	W	RX_SHA-1_HASH_17	XXh
\$72	W	RX_SHA-1_HASH_18	XXh
\$73	W	RX_SHA-1_HASH_19	XXh
\$80 ~ \$CF	W	RX_KSV_FIFO	XXh

### 3.3.1 Register Descriptions

Detailed usage of these IIC registers is described in the following section.

#### 3.3.1.1 TMDS Control Register 0

Table 3-2 TMDS Control Register 0

<b>\$05</b>								
bit	7	6	5	4	3	2	1	0
R								
W	0	0	TMDS_SAMP[5:0]					
Reset:	0	0	0	0	0	1	0	1

TMDS\_SAMP[5:0] — TMDS Sampling Logic Control Parameters

This register is recommended to be programmed with the value 0x09 after the power on sequence if the expected supported TMDS clock frequency is up to 225MHz (1080p, 12 bits deep color). The TMDS\_SAMP[0] is fixed to 1 always.

### 3.3.1.2 TMDS Control Register 1

Table 3-3 TMDS Control Register 1

		\$06							
bit		7	6	5	4	3	2	1	0
R									
W									
Reset:		0	0	0	0	0	0	0	0

**TX\_TERM** — HDMI Transmitter Internal Termination Control

- 1 = Internal Termination is ON
- 0 = Internal Termination is OFF

**DPRE\_EM** — HDMI Transmitter Data Channel Pre-emphasis Control

- 1 = Transmitter Data Channel Pre-emphasis is ON
- 0 = Transmitter Data Channel Pre-emphasis is OFF

**TX\_BW** — HDMI Transmitter PLL Bandwidth Control

- 1 = TX PLL Bandwidth is 1MHz
- 0 = TX PLL Bandwidth is 1.6MHz

**TX\_PEAK** — HDMI Transmitter Active Peaking Control

- 1 = TX Active Peaking is ON
- 0 = TX Active Peaking is OFF

**CPRE\_EM** — HDMI Transmitter Clock Channel Pre-emphasis Control

- 1 = Transmitter Clock Channel Pre-emphasis is ON
- 0 = Transmitter Clock Channel Pre-emphasis is OFF

**RX\_EQ** — HDMI Receiver Equalizer Bias Current Control

- 1 = EQ Bias Current is 125uA
- 0 = EQ Bias Current is 100uA

**RX\_BW** — HDMI Receiver Bandwidth Control

- 1 = 2MHz
- 0 = 4MHz

**RX\_TERM** — HDMI Receiver Clock Channel Termination Control

- 1 = Receiver Clock Channel Termination is 100Ω
- 0 = Receiver Clock Channel Termination is 50Ω

This register is recommended to be programmed with the value 0x80 after the power on sequence if the expected supported TMDS clock frequency is up to 225MHz (1080p, 12 bits deep color). Also, if long cable is supported, the recommended setting will be 0xA0. The transmitter will consume more current if the control bit TX\_TERM is set to 1.

### 3.3.1.3 Control Register 0

**Table 3-4 Control Register 0**

**\$07**

bit	7	6	5	4	3	2	1	0
R	RX_LINK_ON	RX_DE_ON	RX_HDMI	RX_ENC_ON	RX_PU	-	TX_SEL[1:0]	
W	-	-	-	-				
Reset:	-	-	-	-	1	0	0	0

#### RX\_LINK\_ON — Receiver Link On

This bit indicates whether a valid signal appears at the clock input of the receiver port. This bit is valid even when the receiver is powered off.

- 1 = Clock presents at the input of the receiver port
- 0 = No clock is detected at the input of the receiver port

#### RX\_DE\_ON — Receiver DE On

This bit indicates whether DE signal is toggling at the receiver port. This bit is valid only when the receiver is powered on.

- 1 = DE signal is toggling at the receiver port
- 0 = DE signal is not toggling at the receiver port

#### RX\_HDMI — Receiver HDMI signal

This bit indicates whether the receiver port is receiving DVI or HDMI signal

- 1 = HDMI
- 0 = DVI

#### RX\_ENC\_ON — Receiver Decryption On

This bit indicates whether the HDCP decryption is active at the receiver port.

- 1 = HDCP decryption at the receiver port is active
- 0 = HDCP decryption at the receiver port is not active

#### RX\_PU — Receiver Power Down Control Bit

This bit controls the power of the receiver port

- 1 = Normal operation.
- 0 = Power down Mode.

#### TX\_SEL[1:0] — Transmitter Port Select for IIC Access

The 4 transmitter ports share the same IIC register address. This register is used to select which transmitter port is addressed for IIC access.

- 00 = Port 0 is selected
- 01 = Port 1 is selected
- 10 = Port 2 is selected
- 11 = Port 3 is selected

### 3.3.1.4 Control Register 1

Table 3-5 Control Register 1

		\$08							
bit		7	6	5	4	3	2	1	0
R		TX_MUTE	RX_VSYNC	-	-	-	-	TX_ENC_OPT	TX_PU
W			-						
Reset:		0	-	-	0	-	-	0	1

#### TX\_MUTE — Video Mute Transmitter

The bit is used to mute the video for the selected transmitter port.

- 1 = Selected transmitter port is video muted
- 0 = Normal

#### VSYNC — Vertical Sync Status Bit

The VSYNC bit gives the current status of the vertical sync signal received by the receiver.

#### TX\_ENC\_OPT — Transmitter Encryption Option

- 1 = Not affected by RX encryption status.
- 0 = Force not to encrypt if RX is not encrypted.

#### TX\_PU — Transmitter Power Down Control Bit

This bit controls the power of the selected transmitter port

- 1 = Normal operation.
- 0 = Put the selected transmitter port in power down mode.

### 3.3.1.5 Control Register 2

Table 3-6 Control Register 2

		\$09							
bit		7	6	5	4	3	2	1	0
R		-	-	-	-	-	TX_RSEN	TX_HTPLG	-
W							-	-	
Reset:		-	-	-	-	-	-	-	-

#### TX\_RSEN — Transmitter Analog Output Status Bit

The TX\_RSEN bit indicates the analog output status at the selected transmitter port.

- 1 = The selected transmitter analog outputs are connected to the receiver
- 0 = The selected transmitter analog outputs are disconnected

#### TX\_HTPLG — Transmitter Hot Plug Status Bit

The TX\_HTPLG bit indicates the hot plug status at the selected transmitter port.

- 1 = Hot Plug detected at the selected transmitter port.
- 0 = Hot Plug not detected at the selected transmitter port.

### 3.3.1.6 Control Register 3

Table 3-7 Control Register 3

		\$0A							
bit		7	6	5	4	3	2	1	0
R		DK[3:1]			DKEN	-	-	-	-
W		DK[3:1]			DKEN	-	-	-	-
Reset:		1	0	0	0	-	-	-	-

#### DK[3:1] — De-skewing Setting Control Bits

The DK[3:1] setting the clock to data trimming for the timing de-skew among the internal receiver to internal transmitter interface. Eight steps can be selected and the time difference for each step is 200ps. The default is 0 step.

- 000 = -4 step
- 001 = -3 step
- 010 = -2 step
- 011 = -1 step
- 100 = 0 step
- 101 = +1 step
- 110 = +2 step
- 111 = +3 step

#### DKEN — De-Skew (Clock to Data De-skewing) Enable Bit

- 1 = De-Skew Enabled
- 0 = De-Skew Disabled, 0 step is selected

### 3.3.1.7 Control Register 4

Table 3-8 Control Register 4

		\$0E							
bit		7	6	5	4	3	2	1	0
R		-	-	-	-	-	-	TX_EESS	TX_HDMI
W		-	-	-	-	-	-	TX_EESS	TX_HDMI
Reset:		-	-	-	-	-	-	0	1

#### TX\_EESS — Enable Enhanced Encryption Signalling for the selected transmitter port

- 1 = Using Enhanced Encryption Signalling for the selected transmitter port.
- 0 = Using Original Encryption Signalling for the selected transmitter port. This is only valid if the selected transmitter is working in DVI mode (TX\_HDMI = 0).

#### TX\_HDMI — Set HDMI mode for the selected transmitter port

- 1 = Put the selected transmitter port working in HDMI mode. This is valid only if the receiver is receiving HDMI signal.

0 = Put the selected transmitter port working in DVI mode.

### 3.3.1.8 Control Register 5

Table 3-9 Control Register 5

		\$0F							
bit		7	6	5	4	3	2	1	0
R		TX_AKSV_RDY	TX_ENC_ON	-	TX_RPTR	-	-	TX_RI_RDY	TX_ENC_EN
W				-	0	-	-	-	0

#### TX\_AKSV\_RDY — Transmitter AKSV Ready

The TX\_AKSV\_RDY bit indicates whether the HDCP keys and AKSV has been successfully downloaded from external EE or not for the selected transmitter port. This bit is read only.

- 1 = HDCP keys and AKSV has been successfully downloaded from external EE. AKSV is ready for read.
- 0 = HDCP keys and AKSV downloading has not been completed. AKSV is not ready for read.

#### TX\_ENC\_ON — Transmitter HDCP Encryption On

The TX\_ENC\_ON bit indicates whether the HDCP encryption for the selected transmitter port is active or not. This bit is read only.

- 1 = HDCP encryption is active.
- 0 = HDCP encryption is not active.

#### TX\_RPTR — Transmit to Repeater

The TX\_RPTR bit should be set if the receiver side which is connected to the selected transmitter port is a repeater. It should be cleared otherwise.

- 1 = The selected transmitter port is connecting to a repeater.
- 0 = The selected transmitter port is not connecting to a repeater.

#### TX\_RI\_RDY — Transmitter RI Ready

This bit indicates that the first Ri value is available for the selected transmitter port. This bit is read only.

- 1 = First Ri value is available for the selected transmitter port.
- 0 = First Ri value is not available for the selected transmitter port.

#### TX\_ENC\_EN — Transmitter ENC Enable

- 1 = Enable HDCP encryption for the selected transmitter port.
- 0 = Disable HDCP encryption the selected transmitter port.

**3.3.1.9 TX\_BKSV Registers (\$10 ~ \$14) - TX\_BKSV\_1 ~ TX\_BKSV\_5**

**Table 3-10 TX\_BKSV Registers**

\$10 ~ \$14		7	6	5	4	3	2	1	0
bit									
R	TX_BKSV1[7:0] ~ TX_BKSV5[7:0]								
W									
Reset:	-	-	-	-	-	-	-	-	-

These 5 registers for the selected transmitter port should be programmed with receiver’s Key Selection Vector. TX\_BKSV\_1 is the LSB and TX\_BKSV\_5 is the MSB. TX\_BKSV\_5 should be written last, as it triggers the authentication process.

**3.3.1.10 TX\_AN Registers (\$15 ~ \$1C) - TX\_AN\_1 ~ TX\_AN\_8**

**Table 3-11 TX\_AN Registers**

\$15 ~ \$1C		7	6	5	4	3	2	1	0
bit									
R	TX_AN1[7:0] ~ TX_AN8[7:0]								
W									
Reset:	-	-	-	-	-	-	-	-	-

These 8 registers for the selected transmitter port should be programmed with a 64-bit pseudo-random value before triggering the authentication process. TX\_AN\_1 is the LSB and TX\_AN\_8 is the MSB.

**3.3.1.11 TX\_AKSV Registers (\$1D ~ \$21) - TX\_AKSV\_1 ~ TX\_AKSV\_5**

**Table 3-12 TX\_AKSV Registers**

\$1D ~ \$21		7	6	5	4	3	2	1	0
bit									
R	TX_AKSV1[7:0] ~ TX_AKSV5[7:0]								
W									
Reset:	-	-	-	-	-	-	-	-	-

These 5 registers are read only which hold transmitter’s Key Selection Vector for the selected transmitter port. TX\_AKSV\_1 is the LSB and TX\_AKSV\_5 is the MSB. All five bytes should be read from here and then written to the receiver. Byte 5 should be written last to the receiver, as it will trigger authentication there. These 5 registers should not be read until TX\_AKSV\_RDY bit is 1.

### 3.3.1.12 TX\_RI Registers (\$22 ~ \$23) - TX\_RI\_1 ~ TX\_RI\_2

**Table 3-13 TX\_RI Registers**

\$22 ~ \$23

bit	7	6	5	4	3	2	1	0
R	TX_RI_1[7:0] ~ TX_RI_2[7:0]							
W								
Reset:	-	-	-	-	-	-	-	-

These 2 registers hold transmitter’s Ri value for the selected transmitter port. They should be read and compared against the Ri value of the receiver to ensure that the encryption process on the transmitter and receiver is synchronized.

### 3.3.1.13 TX\_M0 Registers (\$25 ~ \$2C) - TX\_M0\_1 ~ TX\_M0\_8

**Table 3-14 TX\_M0 Registers**

\$25 ~ \$2C

bit	7	6	5	4	3	2	1	0
R	TX_M0_1[7:0] ~ TX_M0_8[7:0]							
Reset:	-	-	-	-	-	-	-	-

These 8 registers are read only which hold transmitter’s M0 values which calculated from HDCP engine. These values will be used for SHA calculation.

### 3.3.1.14 RX\_M0\_RDY Register

**Table 3-15 RX\_M0\_RDY Register**

\$40

bit	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	RX_M0_RDY
Reset:	0	0	0	0	0	0	0	0

The RX\_M0\_RDY bit will be set to 1 while the last byte of AKSV is written and the HDCP engine completes the M0 calculation.

### 3.3.1.15 RX\_M0 Registers (\$41 ~ \$48) - RX\_M0\_1 ~ RX\_M0\_8

**Table 3-16 RX\_M0 Registers**

\$41 ~ \$48

bit	7	6	5	4	3	2	1	0
R	RX_M0_1[7:0] ~ RX_M0_8[7:0]							
Reset:	-	-	-	-	-	-	-	-

These 8 registers are read only which hold receiver’s M0 values which calculated from HDCP engine. These values can be read while the RX\_M0\_RDY bit is 1 and can be used for SHA calculation.

### 3.3.1.16 RX\_Bcaps Register

Table 3-17 RX\_Bcaps Register

\$50

bit	7	6	5	4	3	2	1	0
W	HDMI_CAP	REPEATER	FIFO_RDY	FAST	RSVD	RSVD	1.1_FEATURE	FAST_REAUTH
Reset:	1	0	0	1	0	0	0	1

This register is write only. The value writes to this register can be read by the upstream source through the DDC link while the HDCP is invoked.

HDMI\_CAP — HDMI Reserved Bit in HDCP Bcaps register

Value written into this bit will reflect to the HDCP Bcaps register, bit 7, HDMI\_RESERVED bit. Use of this bit is reserved. HDCP receivers not capable of supporting HDMI must clear this bit to 0.

REPEATER — REPEATER Bit in HDCP Bcaps register

Value written into this bit will reflect to the HDCP Bcaps register, bit 6, REPEATER bit.

FIFO\_RDY — READY Bit in HDCP Bcaps register

Value written into this bit will reflect to the HDCP Bcaps register, bit 5, READY bit.

FAST — FAST Bit in HDCP Bcaps register

Value written into this bit will reflect to the HDCP Bcaps register, bit 4, FAST bit.

1.1\_FEATURE — 1.1\_FEATURE Bit in HDCP Bcaps register

Value written into this bit will reflect to the HDCP Bcaps register, bit 1, 1.1\_FEATURE bit. This bit shall set to 0 always.

FAST\_REAUTH — FAST\_REAUTHENTICATION Bit in HDCP Bcaps register

Value written into this bit will reflect to the HDCP Bcaps register, bit 0, FAST\_REAUTHENTICATION bit.

### 3.3.1.17 RX\_Bstatus Registers (\$51 ~ \$52)

Table 3-18 RX\_Bstatus (LSB, [7:0]) Register

\$51

bit	7	6	5	4	3	2	1	0
W	DEV_EXCEED	DEVICE_CNT[6:0]						
Reset:	0	0	0	0	0	0	0	0

**Table 3-19 RX\_Bstatus (MSB, [15:8]) Register****§52**

bit	7	6	5	4	3	2	1	0
W	-	-	-	-	CASC_EXCEED	DEPTH[2:0]		
Reset:	0	0	0	0	0	0	0	0

These 2 bytes registers are write only. The value writes to this register can be read by the upstream source through the DDC link while the HDCP is invoked.

**DEV\_EXCEED** — MAX\_DEVS\_EXCEEDED Bit in HDCP Bstatus register

Value written into this bit will reflect to the HDCP Bstatus register, bit 7, MAX\_DEVS\_EXCEEDED bit.

**DEVICE\_COUNT[6:0]** — DEVICE\_COUNT Bits in HDCP Bstatus register

Value written into this bit will reflect to the HDCP Bstatus register, bit 6 ~ bit 0, DEVICE\_COUNT[6:0] bit.

**CASC\_EXCEED** — MAX\_CASCADE\_EXCEEDED Bit in HDCP Bstatus register

Value written into this bit will reflect to the HDCP Bstatus register, bit 11, MAX\_CASCADE\_EXCEEDED bit.

**DEPTH[2:0]** — DEPTH Bits in HDCP Bstatus register

Value written into this bit will reflect to the HDCP Bstatus register, bit 10 ~ bit 8, DEPTH[2:0] bit.

### 3.3.1.18 RX\_SHA-1\_HASH Registers (§60 ~ §73)

These 20-bytes registers are write only. The value writes to this register can be read by the upstream source through the DDC link while the HDCP is invoked.

**Table 3-20 HDCP SHA-1 Hash Value Registers**

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	reset
0x60	RX_SHA-1_HASH_0								xxh
0x61	RX_SHA-1_HASH_1								xxh
0x62	RX_SHA-1_HASH_2								xxh
0x63	RX_SHA-1_HASH_3								xxh
0x64	RX_SHA-1_HASH_4								xxh
0x65	RX_SHA-1_HASH_5								xxh
0x66	RX_SHA-1_HASH_6								xxh
0x67	RX_SHA-1_HASH_7								xxh
0x68	RX_SHA-1_HASH_8								xxh
0x69	RX_SHA-1_HASH_9								xxh
0x6A	RX_SHA-1_HASH_10								xxh
0x6B	RX_SHA-1_HASH_11								xxh
0x6C	RX_SHA-1_HASH_12								xxh

**Table 3-20 HDCP SHA-1 Hash Value Registers**

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	reset
0x6D	RX_SHA-1_HASH_13								xxh
0x6E	RX_SHA-1_HASH_14								xxh
0x6F	RX_SHA-1_HASH_15								xxh
0x70	RX_SHA-1_HASH_16								xxh
0x71	RX_SHA-1_HASH_17								xxh
0x72	RX_SHA-1_HASH_18								xxh
0x73	RX_SHA-1_HASH_19								xxh

**3.3.1.19 RX\_KSV\_FIFO Registers (\$80 ~ \$CF)**

These 80-bytes registers are write only. The value writes to this register can be read by the upstream source through the DDC link while the HDCP is invoked. The MCU shall write 0x00 to these registers to be the default values. Each KSV list contains 5 bytes registers and the register structure is shown below.

**Table 3-21 KSV\_FIFO Registers**

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	reset
0x80 + 5 * (X-1)	KSVx[7:0]								xxh
0x81 + 5 * (X-1)	KSVx[15:8]								xxh
0x82 + 5 * (X-1)	KSVx[23:16]								xxh
0x83 + 5 * (X-1)	KSVx[31:24]								xxh
0x84 + 5 * (X-1)	KSVx[39:32]								xxh

NOTE: X = downstream device count

# Appendix A Package

Figure A-1 EP9134 Footprint Diagram

